REMARKS

Claims 1 – 19 remain in the application. Claims 9 and 15 – 19 are allowed, claims 1, 13 and 14 were rejected under Section 102(e) while claims 2 – 8 and 10 – 12 were objected to as dependent from rejected claims.

At the outset it is confirmed that the examiner has identified an error in prior argument relating to the positioning of the "conductive layer" recited in the claims. In fact, none of the claims require that the recited "conductive layer" be formed (i) physically between "first and second spaced-apart doped regions [see claim 1]" or (ii) physically between "the first and second regions [see claim 9]" or (iii) physically between "the first source/drain region of each transistor [see claims 15 and 19]." To the extent the undersigned incorrectly characterized the physical positioning of the claimed conductive layer as anything more than that required to effect electrical connection, such argument is expressly withdrawn.

Claim 1 has been amended to fully distinguish over the art of record. Specifically, claim 1 now requires that the third doped region be "monocrystalline." This is to be distinguished from the gate region 20 set forth in Figure 2B of the Chang '367 reference. See Col. 9, lines 49 – 53 in relation to the polysilicon layer 72 shown in Figure 4D. None of the art of record teaches or suggests applicant's combination. Claim 1 has also been amended to delete the word "formed" since this language is not needed to distinguish the invention.

For the above reasons it is submitted that all of the claims are allowable and allowance of the application is requested.

Respectfully,

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